REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-6, 8-9 and 11-15 are pending. Claims 1-6, 8-9 and 11-15 stand rejected.

In this response, claims 1, 5, 6, 11, 13, and 15 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants respectfully submit that the amendments do not add new matter.

Applicants reserve all rights with respect to the applicability of the Doctrine of Equivalents.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1, 8, 9 and 11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,060,033 to Takeuchi ("Takeuchi '033").

Amended claim 1 reads as follows:

> A device comprising:
>
> a substrate having a first conductivity type region, wherein the substrate has inwardly concaved recesses having inflection points;
>
> a gate dielectric formed on the first conductivity region of the substrate between the recesses;
>
> a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;
>
> a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and
>
> a first silicon or silicon alloy layer filling the inwardly concaved recesses that forms a pair of inwardly concaved source/drain regions of a second conductivity type having extensions at the inflection points on opposite sides of said gate electrode, wherein the pair of inwardly concaved source/drain

regions have an abrupt junction between the first conductivity type region and the first silicon or silicon alloy layer filling the inwardly concaved recesses at the inflection points, wherein the pair of the inwardly concaved source/drain regions have extensions at the inflection points determined by the inwardly concaved recesses creating metallurgical inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer, and directly define a first channel region having a first metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and a second channel region having a second metallurgical length between said metallurgical inflection points, wherein said first metallurgical channel length directly beneath said lower portion of said gate electrode is larger than said second metallurgical channel length between said metallurgical inflection points.

(Amended claim 1) (emphasis added)

Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103(a) over Takeuchi '033.

Takeuchi '033 discloses the MOS transistor that comprises a semiconductor substrate 101, an insulation film 102 on the substrate 101, a p-type layer 104 on the semiconductor substrate 101, a gate electrode 105, source drain regions 106 and 109 (**Figure 1h**, col. 3, lines 49-65). More specifically, Takeuchi '033 discloses forming source and drain regions by ion implantation of the impurities into the substrate at opposing sides of gate electrode (**Figures 1(e)** and **1(h)**, col. 4, lines 37-58). Ion implantation results in a smooth, gradual transition (junction) of the impurities [dopants] between the source/drain regions and the substrate.

Applicants submit herewith a Declaration under 37 C.F.R. § 1.132 of inventor Anand Murthy stating that the ion implantation techniques cannot provide a pair of inwardly concaved source/drain regions of a second conductivity type having extensions at the inflection points on opposite sides of said gate electrode, wherein the pair of inwardly concaved source/drain regions have an abrupt junction between the [material of the] first conductivity type region and

the first silicon or silicon alloy layer filling the inwardly concaved recesses at the inflection points, as claimed in amended claim 1. The Declaration under 37 C.F.R. § 1.132 sets forth facts sufficient to show that the junction between the material of the substrate and the material of the silicon or silicon alloy layer that has filled the inwardly concaved recesses including the inflection points (at source/drain extensions) is substantially sharper than the junction between the substrate and source/drain regions formed by the ion implantation techniques.

Accordingly, applicants respectfully submit that Takeuchi '033 does not disclose, teach or suggest a pair of inwardly concaved source/drain regions on opposite sides of the gate electrode, wherein the pair of the inwardly concaved source/drain regions having extensions at the inflection points have an abrupt junction between the first silicon or silicon alloy layer filling the inwardly concaved recesses at the inflection points and the first conductivity type region, as recited in amended claim 1.

Therefore, applicants respectfully submit that amended claim 1 is not obvious over Takeuchi '033 under 35 U.S.C. § 103(a). Applicants accordingly request that Takeuchi '033 be removed from consideration.

Because claims 8, 9, and 11 depend from amended claim 1, and add additional limitations, applicants respectfully submit that claims 8, 9, and 11 are not obvious under 35 U.S.C. § 103(a) over Takeuchi '033.

Claim 2 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033, and further in view of U.S. Patent No. 5,970,351 to Takeuchi ("Takeuchi '351").

Applicants respectfully submit that neither Takeuchi' 033, nor Takeuchi '351 discloses the limitations as discussed with respect to amended claim 1.

It is respectfully submitted that Takeuchi '033 does not teach or suggest a combination with Takeuchi '351, and Takeuchi '351does not teach or suggest a combination with Takeuchi

'033. It would be impermissible hindsight, based on applicants' own disclosure, to combine Takeuchi '033 and Takeuchi '351.

As set forth above, applicants submit herewith a Declaration under 37 C.F.R. § 1.132 of inventor Anand Murthy stating that the ion implantation techniques as taught by Takeuchi '033 cannot provide a pair of inwardly concaved source/drain regions of a second conductivity type having extensions at the inflection points on opposite sides of said gate electrode, wherein the pair of inwardly concaved source/drain regions have an abrupt junction between the first conductivity type region and the first silicon or silicon alloy layer filling the inwardly concaved recesses at the inflection points, as claimed in amended claim 1.

Accordingly, applicants respectfully submit that Takeuchi '033 does not disclose, teach or suggest a pair of the inwardly concaved source/drain regions having extensions at the inflection points that have an abrupt junction between the first silicon or silicon alloy layer filling the inwardly concaved recesses at the inflection points and the first conductivity type region, as recited in amended claim 1.

Takeuchi '351, in contrast, discloses elevated drain/source regions formed on a substrate.

Furthermore, even if the transistor of Takeuchi '033 were combined with the transistor of Takeuchi '351, such a combination would lack a pair of the inwardly concaved source/drain regions having extensions at the inflection points that have an abrupt junction between the first silicon or silicon alloy layer filling the inwardly concaved recesses at the inflection points and the first conductivity type region, as claimed in amended claim 1.

Because claim 2 depends from amended claim 1, and adds additional limitations, applicants respectfully submit that claim 2 is not obvious under 35 U.S.C. § 103(a) over Takeuchi '033, in view of Takeuchi '351.

Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033, in view of U.S. Patent No. 6,057,582 to Choi ("Choi '582").

Applicants respectfully submit that neither Takeuchi '033, nor Choi '582 discloses the limitations as discussed with respect to amended claim 1.

It is respectfully submitted that Takeuchi '033 does not teach or suggest a combination with Choi '582, and Choi '582 does not teach or suggest a combination with Takeuchi '033. It would be impermissible hindsight, based on applicants' own disclosure, to combine Takeuchi '033 and Choi '582.

As set forth above, Takeuchi'033 fails to disclose, teach, or suggest the features discussed with respect to amended claim 1.

Choi '582, in contrast, discloses a transistor having a gate insulating film having thicknesses at both sides thicker than a thickness at a center formed on semiconductor substrate 21.

Furthermore, even if the transistor of Takeuchi '033 were combined with the transistor of Choi '582, such a combination would lack a pair of the inwardly concaved source/drain regions having extensions at the inflection points that have an abrupt junction between the first silicon or silicon alloy layer filling the inwardly concaved recesses at the inflection points and the first conductivity type region, as claimed in amended claim 1.

Because claim 3 depends from amended claim 1, and adds additional limitations, applicants respectfully submit that claim 3 is not obvious under 35 U.S.C. § 103(a) over Takeuchi '033 in view of Choi '582.

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033, in view of Takeuchi '351, and further in view of Choi '582.

As set forth above, neither Takeuchi '033, Takeuchi '351, Choi '582, nor any combination thereof, discloses the discussed limitations of amended claim 1.

Because claim 4 depends from amended claim 1 and add additional limitations, applicants respectfully submit that claim 4 is not obvious under 35 U.S.C. § 103(a) over Takeuchi '033, in view of Takeuchi '351, and further in view of Choi '582.

Claims 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033, and further in view of U.S. Patent No. 5,793,088 to Choi et al. ("Choi '088").

Choi '088, in contrast, discloses controlling the threshold voltage by providing a threshold voltage implant into the edges of the halo regions, and similarly to Takeuchi '033, does not disclose the discussed limitations of amended claim 1.

Because claims 5 and 6 depend from amended claim 1 and add additional limitations, applicants respectfully submit that claims 5 and 6 are not obvious under 35 U.S.C. § 103(a) over Takeuchi '033, in view of Choi '088.

Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033, and further in view of U.S. Patent No. 5,567,966 to Hwang ("Hwang").

It is respectfully submitted that neither Takeuchi '033, nor Hwang disclose the discussed limitations of amended claim 1.

As set forth above, Takeuchi '033 fails to disclose, teach, or suggest the features discussed with respect to amended claim 1.

It is respectfully submitted that Takeuchi '033 does not teach or suggest a combination with Hwang, and Hwang does not teach or suggest a combination with Takeuchi '033. It would be impermissible hindsight, based on applicants' own disclosure, to combine Takeuchi '033 and Hwang.

Takeuchi '033 discloses a transistor having a belt shaped impurity layer. More specifically, Takeuchi '033 discloses that impurities are ion-implanted at opposing sides of gate electrode 105 to form source and drain regions 106 and 109 (**Figures 1(e)** and **1(h)**, col. 4, lines 37-58).

Hwang, in contrast, discloses thinning the channel region by local oxidation and wet etch (Abstract).

Furthermore, even if Takeuchi '033 and Hwang were combined, such a combination would still lack a pair of the inwardly concaved source/drain regions having extensions at the inflection points that have an abrupt junction between the first silicon or silicon alloy layer filling the inwardly concaved recesses at the inflection points and the first conductivity type region, as claimed in amended claim 1.

Because claim 12 depends from amended claim 1, applicants respectfully submit that claim 12 is not obvious under 35 U.S.C. § 103(a) over Takeuchi '033, in view of Hwang.

Claim 13 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of U.S. Patent No. 6,274,894 to Wieczorek et al. ("Wieczorek") in view of Takeuchi '351.

Amended claim 13 includes a pair of inwardly concaved source/drain regions on opposite sides of said gate electrode with extensions directly beneath said lower portion of said gate electrode having an abrupt junction between the silicon germanium alloy filling the inwardly concaved recesses at the inflection points and the first conductivity type region.

Applicants submit herewith a Declaration under 37 C.F.R. § 1.132 of inventor Anand Murthy stating that the ion implantation techniques taught by Takeuchi '033 cannot provide a pair of inwardly concaved source/drain regions on opposite sides of said gate electrode with the inflection points directly beneath said lower portion of said gate electrode having an abrupt

junction between the silicon germanium alloy filling the inwardly concaved recesses at the inflection points and the first conductivity type region, as claimed in amended claim 13. The Declaration under 37 C.F.R. § 1.132 sets forth facts sufficient to show that the junction (boundary) between the material of the substrate and the material of the silicon or silicon alloy layer that has filled the inwardly concaved recesses including the inflection points (at source/drain extensions) is substantially sharper than the boundary between the substrate and source/drain regions formed by the ion implantation techniques, as taught by Takeuchi '033.

Therefore, applicants respectfully submit that Takeuchi '033 fails to disclose the discussed limitations of amended claim 13.

Applicants respectfully submit that none of the references cited by the Examiner discloses the discussed limitations of amended claim 13.

It is respectfully submitted none of the references teach or suggest a combination with each other. It would be impermissible hindsight, based on applicants' own disclosure, to combine Takeuchi '033, Wieczorek and Takeuchi '351.

Takeuchi '351 discloses elevated drain/source regions formed on a substrate (Abstract).

Wieczorek, in contrast, discloses forming low-bandgap source and drain regions for MOS transistors. More specifically, Wieczorek discloses forming trenches (52) in the substrate (**Figure 7**), forming the SiGe layer 54 in the trenches (**Figure 8**), and then filling the trenches with the semiconductor portions 56 (**Figure 9**) (col. 11, line 15-col. 12, line 50).

Furthermore, even if the transistor of Takeuchi '033 were combined with the transistors of Wieczorek and Takeuchi '351, such a combination would still lack a pair of inwardly concaved source/drain regions on opposite sides of said gate electrode with extensions directly beneath said lower portion of said gate electrode having an abrupt junction is formed between

the silicon germanium alloy filling the inwardly concaved recesses at the inflection points and the first conductivity type region, as recited in amended claim 13.

Therefore, applicants respectfully submit that claim 13 is not obvious under 35 U.S.C. § 103(a) over Takeuchi '033, in view of Wieczorek, and further in view of Takeuchi '351.

Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of Wieczorek in view of Takeuchi '351 as applied to claim 13 above, and further in view of Choi '582.

As set forth above, neither Takeuchi '033, Wieczorek, Takeuchi '351, Choi '582, nor a combination thereof, discloses the discussed limitations of amended claim 13.

Because claim 14 depends from amended claim 13, and adds additional limitations, applicants respectfully submit that claim 14 is not obvious under 35 U.S.C. § 103(a) over Takeuchi '033, in view of Wieczorek, in view of Takeuchi '351, and further in view of Choi '582.

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of Wieczorek.

Amended claim 15 includes a pair of inwardly concaved source/drain regions of a second conductivity type having a concentration of impurities in a range of $1x10^{18}/cm^3$ – $3x10^{21}/cm^3$ at opposite sides of said gate electrode with extensions directly beneath the lower portion of the gate electrode having an abrupt junction between the first conductivity type region and the silicon-germanium layer filling the inwardly concaved recesses at the inflection points.

Applicants respectfully submit that none of the references cited by the Examiner discloses such limitations of amended claim 15.

Applicants submit herewith a Declaration under 37 C.F.R. § 1.132 of inventor Anand Murthy stating that the ion implantation techniques taught by Takeuchi '033 cannot provide a pair of inwardly concaved source/drain regions of a second conductivity type having a concentration of impurities in a range of $1x10^{18}/cm^3 - 3x10^{21}/cm^3$ at opposite sides of said gate electrode with extensions directly beneath the lower portion of the gate electrode having an abrupt junction between the first conductivity type region and the silicon-germanium layer filling the inwardly concaved recesses at the inflection points, as claimed in amended claim 15.

It is respectfully submitted none of the references teach or suggest a combination with each other. It would be impermissible hindsight, based on applicants' own disclosure, to combine Takeuchi '033 and Wieczorek.

Takeuchi '033 discloses a transistor having a belt shaped impurity layer.

Wieczorek, in contrast, discloses forming low-bandgap source and drain regions for MOS transistors.

Furthermore, even if the transistor of Takeuchi '033 were combined with the transistor of Wieczorek, such a combination would still lack a pair of inwardly concaved source/drain regions of a second conductivity type having a concentration of impurities in a range of $1x10^{18}/cm^3 - 3x10^{21}/cm^3$ at opposite sides of said gate electrode with extensions directly beneath the lower portion of the gate electrode having an abrupt junction between the first conductivity type region and the silicon-germanium layer filling the inwardly concaved recesses at the inflection points, as recited in amended claim 15.

Therefore, applicants respectfully submit that amended claim 15 is not obvious under 35 U.S.C. § 103(a) over Takeuchi '033, in view of Wieczorek.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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Date: October 31, 2007

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